

REMARKS

In the Office Action of March 20, 2007, the Examiner (1) objected to specification; (2) objected to drawings; (3) objected to claim 17; (4) rejected claims 1-8, 17, 19, 20 and 22 as allegedly double patenting over claims 1-8 and 18-21 of copending Application No. 11/105,755; (5) rejected claims 1-4, 6, 10, 16-17, 19-20 and 22 as allegedly anticipated by U.S. Patent No. 5,644,597 (“Ueda”); (6) rejected claims 1, 7 and 10 as allegedly anticipated by U.S. PGPub No. 2003/0133424 (“Liang et al.”); and (7) rejected claim 9 as allegedly obvious over Ueda and U.S. Patent No. 6,763,074 (Yang). The Examiner also concluded that dependent claims 11-15, 18 and 21 would be allowed if rewritten in independent form.

With this response, Applicants amend claim 17. Applicants believe that the pending claims are allowable over the art of record and respectfully request reconsideration.

I. SPECIFICATION OBJECTIONS

With respect to paragraph [0044], applicants present plurality amendments to correct the reference numbers to Figure 2d. No new matter is added.

II. DRAWING OBJECTIONS

With respect to paragraph [0045] and [0046], applicants present plurality amendments to correct reference numbers to Figure 3 and 4. Therefore, Applicants respectfully requests that the objections should be withdrawn.

III. CLAIM OBJECTIONS

Applicants amend claim 17 to fix an antecedent basis error, and not define over any prior art or narrow the scope of the claim.

IV. DOUBLE PATENTING REJECTION

Claims 1-8, 17, 19, 20 and 22 stand rejected as allegedly double patenting over claims 1-8, and 18-21 of copending Application No. 11/105,755. The applicants request that the double patenting rejection of claims 1-8, 17, 19, 20 and 22 be held in abeyance until one of the copending application is otherwise in condition for allowance and then, if appropriate consider the double patenting issue with regard to the later allowed of the two copending applications.

V. ART BASED REJECTIONS

A. Claim 1

Claim 1 stands rejected as allegedly anticipated by Ueda U.S. Patent No. 5,644,597. Ueda is directed towards an adaptive equalizer and adaptive diversity equalizer. (Ueda Title). In particular, Ueda teaches an adaptive equalizer including a decision feedback equalizer and a linear adaptive equalizer. (Ueda Col. 45, lines 52-67 to Col. 46, lines 1-40). Further, Ueda appears to teach a delay measuring circuit, comprising a correlator, for determining multipath propagation characteristic for a channel. (Ueda Abstract). The correlator outputs a correlation value, which is used to decide if either one of the decision feedback adaptive equalizer and the linear adaptive equalizer should be operated. (Ueda Col. 46, lines 57-63). Therefore, Ueda appears to teach configuration of the adaptive equalizers; however, Ueda is silent as to configuration of the operational blocks interconnected to the equalizers.

Claim 1, by contrast, specifically recites, “a control mechanism that **configures the adaptive equalizers and operational blocks** according to different signal delay profiles.” Applicants respectfully submit that Ueda does not expressly or inherently teach such a system. Ueda may disclose configuration of the adaptive equalizers; however, Ueda is silent as to configuration of the operational blocks interconnected to the equalizers. Thus, Ueda fails to expressly or inherently teach “a control mechanism that **configures the adaptive equalizers and operational blocks** according to different signal delay profiles.”

Claim 1 also stands rejected as allegedly anticipated by Liang U.S. PGPub No. 2003/0133424. Liang is directed towards a path diversity equalization CDMA downlink receiver. (Liang Title). In particular, Liang appears to teach an equalization receiver in a mobile station including a code generator, an intelligent cluster analyzer, and multiple short equalizers. (Liang Paragraph [0074]). The intelligent cluster analyzer receives power delay profile estimate from the code generator, and generates information regarding the number of short equalizers. (Liang Paragraph [0075]). Therefore, Liang appears to teach selecting a number of short equalizers; however, Liang is silent as to configuration of the operational blocks interconnected to the equalizers.

Claim 1, by contrast, specifically recites, “a control mechanism that **configures the adaptive equalizers and operational blocks** according to different signal delay profiles.”

Applicants respectfully submit that Liang does not expressly or inherently teach such a system. Therefore, Liang may teach selecting a number of short equalizers; however, Liang is silent as to configuration of the operational blocks interconnected to the equalizers. Thus, Liang fails to expressly or inherently teach “a control mechanism that **configures the adaptive equalizers and operational blocks** according to different signal delay profiles.”

Based on the foregoing, Applicant respectfully submits that claim 1, and all claims which depend from claim 1 (claims 2-9), should be allowed.

B. Claim 10

Claim 10 stands rejected as allegedly anticipated by Ueda. Claim 10 specifically recites, “operating two or more adaptive equalizers, computational resources of the two or more adaptive equalizers, and **operational blocks interconnecting said two or more adaptive equalizers** according to said attributes of the multi-path signal profile.” Applicants respectfully submit that Ueda does not expressly or inherently teach such a system. Therefore, Ueda may disclose configuration of the adaptive equalizers; however, Ueda is silent as to configuration of the operational blocks interconnected to the equalizers. Thus, Ueda fails to expressly or inherently teach “operating two or more adaptive equalizers, computational resources of the two or more adaptive equalizers, and **operational blocks interconnecting said two or more adaptive equalizers** according to said attributes of the multi-path signal profile.”

Claim 10 stands rejected as allegedly anticipated by Liang. Claim 10 specifically recites, “operating two or more adaptive equalizers, computational resources of the two or more adaptive equalizers, and **operational blocks interconnecting said two or more adaptive equalizers** according to said attributes of the multi-path signal profile.” Applicants respectfully submit that Liang does not expressly or inherently teach such a system. Therefore, Liang may disclose configuration of the adaptive equalizers; however, Liang is silent as to configuration of the operational blocks interconnected to the equalizers. Thus, Liang fails to expressly or inherently teach “operating two or more adaptive equalizers, computational resources of the two or more adaptive equalizers, and **operational blocks interconnecting said two or more adaptive equalizers** according to said attributes of the multi-path signal profile.”

Based on the foregoing, Applicant respectfully submits that claim 10, and all claims which depend from claim 10 (claims 11-16), should be allowed.

C. Claim 17

Claim 17 stands rejected as allegedly anticipated by Ueda. Applicants amend claim 17 to fix an antecedent basis error, and not define over any prior art or narrow the scope of the claim. Claim 17 specifically recites, “means for **configuring** the two or more adaptive equalizers and **operational blocks** according to attributes of the signal profile.” Applicants respectfully submit that Ueda does not expressly or inherently teach such a system. Therefore, Ueda may disclose configuration of the adaptive equalizers; however, Ueda is silent as to configuration of the operational blocks interconnected to the equalizers. Thus, Ueda fails to expressly or inherently teach “means for **configuring** the two or more adaptive equalizers and **operational blocks** according to attributes of the signal profile.”

Based on the foregoing, Applicant respectfully submits that claim 17, and all claims which depend from claim 17 (claims 18-22), should be allowed.

VI. CONCLUSION

In course of the foregoing discussions, Applicant may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and cited art which have yet to be raised, but which may be raised in the future.

**Appl. No. 10/699,707
Amdt. dated July 20, 2007
Reply to Office Action of March 20, 2007**

Applicant respectfully requests reconsideration and that a timely Notice of Allowance be issued in this case. If the Examiner feels that a telephone conference would expedite the resolution of this case, he is respectfully requested to contact the undersigned. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to the Texas Instruments, Inc. Deposit Account No. 20-0668.

Respectfully submitted,

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